REMARKS

Status of the Claims

Claims 1, 3, 4, 6-8, and 10 are currently present in the Application, and claim 1 is an independent claim. Claims 1, 4, 8, and 10 have been amended, and claims 2, 5, 9, and 11-30 have been canceled. Applicants are not conceding that the subject matter encompassed by claims 1-30 prior to this Amendment, is not patentable over the cited by the Examiner. Claims 1, 4, 8, and 10 were amended, and claims 2, 5, 9, and 11-30 were canceled solely to facilitate expeditious prosecution of the remaining claims. Applicants respectfully reserve the right to pursue claims, including the subject matter encompassed by claims 1-30, prior to this Amendment, and other claims, in one or more continuation and/or divisional Applications.

Support for the amendments to the claims is found in Applicants' specification on page 47, line 25 through page 52, line 27 (also see Figures 43A, 43B, 44, and 45). Further support is found in claim 9, as originally filed. No new matter has been added as a result of the amendments to the claims.

Examiner Interview

Applicants wish to thank the Examiner for the courtesy extended to Applicants' attorney during a telephone interview on June 6, 2008. During the interview, Applicants' attorney proposed amending the independent claims to clarify that the first processor and the second processor are heterogeneous processors, and also to clarify the relationship between the first and second processors. The Examiner indicated that he would do further searching upon receipt of Applicants' formal Response. No agreement was reached regarding the claims during the interview.

Information Disclosure Statements

Applicants note that the Information Disclosure Statements filed on October 2, 2007 and July 16, 2007 do not appear to have been considered by the Examiner. Applicants respectfully request that the Examiner consider the Information Disclosure Statements filed on October 2, 2007 and July 16, 2007, and return initialed copies of the Form PTO-1449 for each of these with the next Action.

Claim Rejections – Alleged Obviousness Under 35 U.S.C. § 103

Claims 1-30 stand rejected under 35 U.S.C. § 103(a) as being unptatentable over Antoniu et al., "The Hyperion System: Compiling Multithreaded Java Bytecode for Distributed Execution," (hereinafter Antoniu) in view of Gun Sirer et al., "Design and Implementation of a Distributed Virtual Machine for Networked Computers," (hereinafter Gun). Applicants respectfully traverse the rejections under 35 U.S.C. § 103.

Note that claims 2, 5, 9, and 11-30 have been canceled, and therefore the rejections to these claims are now moot.

The Office Action cites Antoniu as disclosing heterogeneous processors within a computer system (see Office Action, pages 2-3). Applicants respectfully submit that Antoniu does not teach or suggest a first processor and a second processor where "the first processor and the second processor are heterogeneous processors, wherein the first processor executes a first instruction set and wherein the second processor executes a second instruction set," as taught and claimed by Applicants. Antoniu states that "[u]pon arrival at the server, the bytecode is translated for native execution on the processors of the server" (Antoniu, page 1281). When referring to "the processors of the server," Antoniu does not state that these are heterogeneous processors, nor does Antoniu make any reference to a first processor executing a first instruction set and a second processor executing a second instruction set, as taught and claimed by Applicants. The Office Action further cites Antoniu at page 1290 (see Office Action, page 3). The cited section of Antoniu discusses running programs on an 8-node cluster of 200 MHz Pentium Pro processors, and then running the same programs on a 4-node cluster of 450 MHz Pentium II processors. In both cases, the cluster of processors is a homogeneous cluster, as each processor in the cluster is of the same type, i.e. each processor in the cluster is a 200 MHz Pentium Pro processor in the 8-node cluster case and each processor in the cluster is a 450 MHz Pentium II processor in the 4-node cluster case. In each cluster, the processors in the cluster use the same instruction set. Antoniu does not teach or suggest running its programs in a heterogeneous system, as taught and claimed by Applicants.

The Office Action further cites Gun as disclosing a heterogeneous cluster (see Office Action, page 3). While Gun does discuss a distributed virtual machine for networked computers (see Gun, Abstract and also pages 205-207), Gun does not teach or suggest a system with "a common memory, the common memory accessible by a first processor and a second processor, wherein the first processor and the second processor are heterogeneous processors, wherein the first processor executes a first instruction set and wherein the second processor executes a second instruction set, and wherein the first processor includes a first local memory accessible to the first processor and the second processor includes a second local memory accessible to the second processor," as taught and claimed by Applicants. Gun is concerned with a system of networked computers and not with heterogeneous processors within the same computer system, each with its own local memory and instruction set, and also sharing a common memory, as taught and claimed by Applicants.

Applicants have amended independent claim 1 to clarify that the second processor processes the software code data by "processing the virtual machine code at the second processor using the virtual machine engine." This processing, by the second processor, which is specifically claimed to execute a second instruction set, results in executable instructions, "the executable instructions comprising instructions from the first instruction set and capable of being executed by the first processor." In other words, the second processor processes the virtual machine code in order to produce instructions that are not capable of being executed via its own instruction set, but rather are capable of being executed by the first processor using the first processor's instruction set. Neither Antoniu nor Gun appears to disclose this type of processing.

Applicants have also amended independent claim 1 to clarify the interactions between the first and second heterogeneous processors. Applicants teach and claim "loading a virtual machine engine into a common memory." This virtual machine engine is then loaded, on an as-needed basis, into the second processor's local memory after the second processor has received the code processing request. Neither Antoniu nor Gun teaches or suggests "in response to receiving the code processing request,

loading, at the second processor, the virtual machine engine from the common memory into the second local memory," as taught and claimed by Applicants.

Applicants further teach and claim that the first processor writes "a code processing request into a mailbox associated with the second processor." Neither Antoniu nor Gun appears to disclose a mailbox associated with a processor.

Based on the above discussion, Applicants respectfully submit that neither Antoniu nor Gun teach or suggest many of the elements of independent claim 1. Therefore, independent claim 1, and the claims which depend from it, are patentable over Antoniu in view of Gun, and Applicants respectfully request that they be allowed.

Conclusion

As a result of the foregoing, it is asserted by Applicants that the remaining claims in the Application are in condition for allowance, and Applicants respectfully request an early allowance of such claims.

Applicants respectfully request that the Examiner contact the Applicants' attorney listed below if the Examiner believes that such a discussion would be helpful in resolving any remaining questions or issues related to this Application.

Respectfully submitted,

By /Leslie A. Van Leeuwen, Reg. No. 42,196/

Leslie A. Van Leeuwen, Reg. No. 42,196
Van Leeuwen & Van Leeuwen
Attorneys for Applicant
Telephone: (512) 301-6738
Facsimile: (512) 301-6742